1. (Previously Presented) A method for initializing a computer system, comprising the steps of:

sensing a command signal to boot the computer system;

generating a first control signal to initialize a boot process;

generating a second control signal to initialize a programmable logic device prior to completion of the initialization of the boot process; and

booting the computer system using the initialized programmable logic device to perform input/output (I/O) or DMA (direct memory access) transfers.

2. (Original) The method of claim 1, wherein the second control signal causes the programmable logic device to self-load logic code from a memory device.

3. (Original) The method of claim 1, wherein the second control signal causes a logic device to load logic code into the programmable logic device.

4. (Original) The method of claim 1, further comprising the step of sensing power to ensure power stability prior to generating the second control signal.

5. (Original) The method of claim 1 wherein the method steps are performed by a boot management circuit that manages the boot process.

6. (Original) The method of claim 1, further comprising the steps of generating a third control signal to indicate the type of boot process commanded.

7. (Original) The method of claim 6, wherein the type of boot process comprises one of a cold boot and a warm boot.

8. (Previously Presented) A program storage device readable by a machine, tangibly embodying a program of instructions executable by the machine to perform method steps for initializing a computer system, the method steps comprising:

sensing a command signal to boot the computer system;

generating a first control signal to initialize a boot process;

generating a second control signal to initialize a programmable logic device prior to completion of the initialization of the boot process; and

booting the computer system using the initialized programmable logic device to perform input/output (I/O) or DMA (direct memory access) transfers.

9. (Original) The program storage device of claim 8, wherein the second control signal causes the programmable logic device to self-load logic code from a memory device.

10. (Original) The program storage device of claim 8, wherein the second control signal causes a logic device to load logic code into the programmable logic device.

11. (Original) The program storage device of claim 8, further comprising instructions for sensing power to ensure power stability prior to generating the second control signal.

12. (Original) The program storage device of claim 8, further comprising instructions for generating a third control signal to indicate the type of boot process commanded.

13. (Original) The program storage device of claim 12, wherein the type of boot process comprises one of a cold boot and a warm boot.

14. (Currently Amended) A circuit for managing initialization of a computer system, comprising:

a first sense circuit for sensing power-up and ensuring power stability;

a second sense circuit for sensing a command signal to boot the computer system;

a control circuit for generating a control signal in response to sensing of a command signal, to initialize a programmable logic device in advance of a boot process to perform input/output (I/O) or DMA (direct memory access) transfers for the boot process; and

a state machine for outputting a flag indicative of the type ~~of the type~~ of boot process commanded.

15. (Original) The circuit of claim 14, further comprising a first waveshaping circuit, operatively coupled to the first sense circuit, for generating a first pulse signal that is utilized to generate the control signal in response to a cold boot command.

16. (Original) The circuit of claim 15, wherein the first waveshaping circuit comprises a falling edge differentiator circuit.

17. (Original) The circuit of claim 14, further comprising a second waveshaping circuit, operatively coupled to the second sense circuit, for generating a second pulse signal that is utilized to generate the control signal in response to a warm boot command.

18. (Original) The circuit of claim 17, wherein the second waveshaping circuit comprises a rising edge differentiator circuit.

19. (Previously Presented) A system for initializing a computer, comprising:

a boot storage device for storing initialization program code for initializing a computer during a boot process; and

a boot device adapter, operatively interfaced with the boot storage device, for accessing the initialization program code from the boot storage device in response to a request from the computer system; wherein the boot device adapter comprises:

a programmable logic device; and

a boot control circuit for generating a control signal to initialize the programmable logic device in advance of the boot process to perform input/output (I/O) or DMA (direct memory access) transfers for the boot process.

20. (Original) The system of claim 19, further comprising a memory device for storing logic code associated with the programmable logic device.

21. (Original) The system of claim 20, wherein the memory device resides in one of the boot device adapter, the computer system and both.

22. (Original) The system of claim 20, wherein the programmable logic device self-loads the logic code from the memory device in response to the control signal.

23. (Original) The system of claim 22, wherein the logic code comprises non-volatile logic code residing in memory on the boot storage device.

24. (Previously Presented) A system for initializing a computer, comprising:

a boot storage device for storing initialization program code for initializing a computer during a boot process; and

a boot device adapter, operatively interfaced with the boot storage device, for accessing the initialization program code from the boot storage device in response to a request from the computer system; wherein the boot device adapter comprises:

a programmable logic device; and

a boot control circuit for generating a control signal to initialize the programmable logic device in advance of the boot process; and

a digital signal processor (DSP) that initializes the programmable logic device in response to the control signal.

25. (Original) The system of claim 24, wherein the boot control circuit comprises a state machine that outputs a flag signal indicative of the type of boot process commanded.

26. (Original) The system of claim 24, wherein the DSP processes the flag signal to determine whether to re-initialize the programmable logic device, if the flag signal indicates a warm boot process.

27. (Original) The system of claim 24, wherein the DSP resides on the boot device adapter.

28. (Original) The system of claim 24, wherein the DSP is operatively connected to the programmable logic device through a dedicated bus of the DSP.

29. (Original) The system of claim 28, wherein the dedicated bus comprises a communications port.

30. (Original) The system of claim 24, wherein the DSP retrieves logic code associated with the programmable logic device from a memory device residing on the boot device adapter.

31. (Original) The system of claim 30, wherein the memory device stores logic code associated with the DSP.